Reliable Low Voltage Circuit Design Techniques

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***Abstract*— In this paper, non-conventional circuit design techniques has been reviewed. The techniques discussed are widely used for realizing low voltage low power analog circuits. The discussed techniques in this paper are: Bulk Driven, Floating and Quasi-floating Gate followed by operating of Bulk Driven MOSFET in Floating and Quasi-floating Gate mode. In all the approach, the threshold voltage restriction is removed or reduced from the input signal path thereby reducing the power consumption. However, the adverse effect lies is terms of reduced performance parameters of MOSFET compared to conventional gate driven MOSFET parameters as shown in this paper through simulation results. The comparative analysis of MOSFET parameters results in encouragement of two approaches: Quasi-floating Gate and Bulk Driven Quasi-floating Gate MOSFET. Each of these approaches has its advantage in specific domains. Further in this paper, an Operational Transconductance Amplifier is proposed which use the Bulk Driven Quasi-floating Gate MOSFET technique and the same is amplifier under similar conditions is also realized using Bulk Driven MOSFET so as to highlight the advantage of Bulk Driven Quasi-floating Gate MOSFET over Bulk Driven MOSFET. All the performances metrics are achieved with the help of HSpice simulator using MOSFET models of 180nm technology provided by UMC.**

***Index Terms*— Bulk Driven, Floating gate, Quasi-floating gate, transconductance, low power.**

I. INTRODUCTION

The trend of CMOS technology scaling towards increasing density of components on chip and prolonging lifespan of battery powered portable and implantable medical devices has pushed the research to adopt hybrid techniques for realizing low voltage (LV) low power (LP) circuits. Though such techniques provide promising results but at the same time shows degraded characteristics [1, 2]. In modern technology era, especially for low voltage analog circuits the threshold voltage has been continuously an obstacle during design requirements.

In this regard, the minimum supply voltage cannot be scaled below the threshold voltage of MOSFET. Few widely adopted low voltage (LV) low power (LP) techniques which have proved its potential are subthreshold (weak inversion) region [3], level shifter technique [4], Bulk Driven technique [5], Floating Gate (FG) structure [6], Quasi-floating Gate (QFG) structure [7, 8], and Bulk driven floating/quasi-floating Gate (BDFG/BDQFG) structure [9]. These LV LP techniques are categorized as non-conventional technique. Depending upon the desired performance parameter enhancement, the selection of technique is done. The main disadvantage of using these techniques is visible in low transconductance compared to gate driven (GD) MOSFET which results in low bandwidth analog circuits. The key features of FG and QFG MOST lies in terms weighted sum operation of multi input capacitive connection and makes the threshold scalable favouring low voltage operation. However, comparing the features of FG with QFG MOST, the QFG MOST gained potential interest.

The main disadvantage with FG MOST is the initial charge trapping at FG node and also the DC convergence issue which is not the case with QFG MOST. Also the QFG MOST shows improved gain-bandwidth product and wide-band operation over FG MOST. Besides floating gate technology, another widely acceptable low power approach is using the BD MOST which has gained popularity due to simple structure. Also the technique best suits to medical devices since the biological signals are of low amplitude (in range of micro to milli volts) and low frequency range (fraction of a hertz to kilohertz) [10].

However, the poor body transconductance of BD MOST forces its application limited to low gain low frequency application. In this context, BDFG/BDQFG technique improved the frequency characteristics of BD MOST. These structures combine the features of BD with FG/QFG MOSFET [9] due to which transconductance is increased and also the frequency range. The paper is organised as follows. Section II covers the brief discussion on non-conventional circuit design techniques highlighting the important features. The supporting simulations for these techniques are shown in Section III followed by conclusion in Section IV.

II. LITERATURE REVIEW

In this section, the low voltage low power techniques namely: BD, FG, QFG, BDFG and BDQFG are reviewed.

Bulk Driven (BD) MOSFET

The conventional MOS transistor (MOST) is a four terminal device, i.e. drain (D), gate (G), source (S) and bulk (B) whose fourth terminal, the bulk is usually connected either negative/positive supply for N-channel/P-channel transistor, respectively, or to their respective source terminal. But by using the bulk-terminal as a signal input instead of connecting it to any of the supply voltage or source terminal, the threshold voltage limitation can be removed. The BD MOST based circuit was first reported in [11].

The working of BD is similar to that of junction field effect transistor (JFET). Moreover, since the BD MOST acts

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as a depletion type device, it can be operated under negative, zero, or even slightly positive biasing conditions [12]. As in GD MOST, the gate-to-source voltage controls the drain current likewise in BD MOST threshold voltage becomes the function of the bulk-to-source voltage which controls the drain current.

The DC bias voltage at gate terminal forms the conduction channel of MOSFET which makes the input pathway free from threshold and the input signal applied at bulk is able to modulate the drain-to-source current even with very low ampitude of signal. Using BD, the circuits can be easily realized for sub-volt supplies. The most significant drawback related to the BD is its small body transconductance (g_{mb}) which is 3 to 5 times smaller than gate transconductance (g_m) and poor transition frequency (f_T) [13].

Despite of this drawback, BD has gained its potential interest by battery-powered medical devices. Since bio-signals are small in amplitude and have low frequency range in KHz, the low value of g_{mb} of BD helped to realize Gm-C low pass filter for bio-signal processing [14]. The literature survey has shown that most of the recent research articles are based on BD [15, 16] where by using appropriate circuit design techniques the BD MOST drawbacks have been alleviated. The symbol of GD and BD NMOST are shown in Fig. 1(a) and (b) respectively.

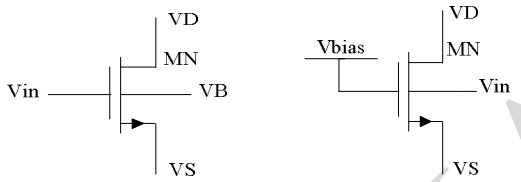

Fig 1. Symbol of N-channel: (a) GD MOST; (b) BD MOST

Unlike the GD technique the input V_{in} is fed to the bulk terminal and a constant DC bias voltage V_{bias} is applied at the gate terminal. The overall advantage and disadvantage using BD MOST is summarized as follows:

Advantage:

- Input pathway free from threshold voltage
- Wide input common mode range
- Rail-to-rail operation
- Less complex

Disadvantages:

- Poor transconductance
- Isolated bulk require special Process
- Poor frequency response
- Degraded Latch up Immunity

Floating Gate (FG) MOSFET

The very first application of FG MOST was used to store data in EPROM, EEPROM and flash memories [17]. During the last decades, a number of different applications have revealed its applicability in many other different fields besides its programmability feature. The best use of FGMOS has been found for tuning in analog CMOS amplifiers to achieve high linearity and also remove offset errors which occur due to device mismatch [18]. Based on FG MOST, various articles have been reported in literature focused on realizing low voltage low power circuits [19]. The input capacitor in FGMOS transistors creates a capacitor divider network which causes the input signal to attenuate and hence increases the linearity.

Unlike the conventional GD MOST, the FG MOST has its gate electrically isolated from inputs, i.e. gate in floating state such that there are no resistive connections to its inputs. The FG is fabricated using the gate electrode (poly1) layer completely surrounded by two SiO2 insulator layers (upper and lower) and thus get electrically isolated from the rest of the device contacts. The inputs are then deposited on top of upper SiO2 layer and fabricated using a second layer of polysilicon (poly2).

This creates a capacitive connection between the FG and actual inputs. Using capacitive connections a number of secondary gates/inputs can be deposited above the floating gate (FG) and the architecture got popularity with the name multi-input FG MOST device. These capacitor values are determined by the sizes of the input electrodes and are varied according to the requirements. In terms of its DC operating point, the FG acts as a floating node. The schematic for an N-input N-channel FGMOS transistor is shown in Fig. 2.

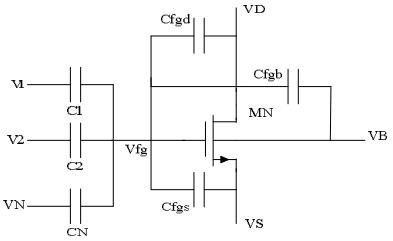

Fig 2. Schematic of N-input N-channel FG MOST

The gate of MOST MN is at floating state (V_{fg}) under DC condition whereas it is capacitively connected to inputs $V_{1...N}$ via second layer of ploysilicon. The input capacitor $C_{1...N}$ formed is referred as poly-poly (PIP) capacitor while others $(C_{fgs}, C_{fgd}, C_{fgb})$ are the parasitic capacitance associated the floating gate node. The overall advantage and disadvantage using FG MOST is summarized as follows:

Advantage:

- Reduced the circuit complexity
- Threshold voltage scalable
- Low voltage operation
- Simplify the signal processing
- Inherently act as level shifter

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Disadvantage:

- Large chip area
- Poor transconductance
- Increased conductance
- Charge trapping

Quasi-floating Gate (QFG) MOSFET

The QFG MOST circuits are wide-band ac coupled circuits which operate at much lower supply than conventional GD MOST [20]. While working with FGMOS transistor two major issues were encountered: (i) Initial charge trapping at FG node; and (ii) Poor gain-bandwidth (GB) product. In context above issues, a new modified architecture of FGMOS was proposed very much similar to FGMOS named as QFG MOST.

In QFGMOS device, a large value resistor is used as a replacement for bias capacitor. Such high value resistor is realized by leakage resistance $\left(R_{large}\right)$ of a reverse biased junction of MOST operating in cut-off region. This high value leakage resistance connects the FG node weakly to the desired DC level and this changes the gate potential floating state to quasi-floating. Moreover, the small value of parasitic gate-to-drain capacitance of cut-off MOST used does not degrade the GB product as much like in case of FG MOST [21]. The capacitor divider at input helped in design of very linear programmable circuits like CMOS OTA to implement tunable MOS resistors [22], GM-C filter [23], current conveyor [24], current mirror [25] etc. The schematic of an N-channel QFGMOS along with its parasitic capacitances is shown in Fig. 3. The P-channel MOST (MP) has its gate connected to positive supply rail VDD which makes it to work in cut-off region and realize a very high value resistance R_{large}.

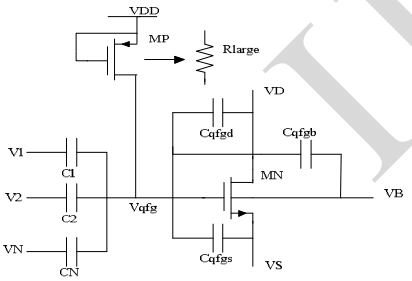

Fig 3. Equivalent circuit of N-input N-channel QFG MOST

The effective gate potential for QFG MOST under ac in s-domain is expressed as

$$V_{qfg} = \left(\frac{sR_{large}C_{T,QFG}}{1+sR_{large}C_{T,QFG}}\right) \left(\frac{\sum_{i=1}^{n} C_i V_i + C_{qfgs}V_S + C_{qfgd}V_D + C_{qfgb}V_B}{C_{T,QFG}}\right) \quad (1)$$

where $C_{T,QFG} = \sum_{i=1}^{n} C_i + C_{qgs} + C_{qgd} + C_{qgb} + C_{gd,MP}$, C_i is the coupling capacitor of the ith input branch whereas C_{gs}, C_{gd}, C_{gb} are the associated parasitic of NMOS to the floating gate, and $C_{gd,MP}$ is the parasitic capacitance associated with PMOS transistor MP. As observed the equation (1) represents a high-pass filter with cut-off frequency of given by $f_0 = 1/2\pi R_{large}C_{T,QFG}$. So, using QFGMOS, applications where very low cut-off frequency is required generally below 1 Hz can be easily achieved by tuning R_{large}, for example in bio-amplifiers. The overall advantage and disadvantage using QFG MOST over FG MOST is summarized as follows:

Advantage:

- Prevent initial charge trapping issue
- Low voltage operation
- Less silicon area compared to FG MOSFET
- Acts as HPF supporting cut-off frequency below 1 Hz
- Improved gain-bandwidth over FG MOSFET

Disadvantage:

- Output conductance slightly higher over FG MOSFET
- Increased static power dissipation

Bulk Driven Floating Gate (BDFG) MOSFET

The bulk-driven floating gate (BDFG) MOST is similar to that of BD MOST, except the difference lies in gate-node potential. In BDFG instead of applying gate to a fixed DC potential, it is configured in floating state. The structure overcomes the major drawback of BD MOST, i.e. low transconductance and poor frequency response. The schematic of an N-channel BDFG MOST along with its parasitic capacitances is shown in Fig. 4.

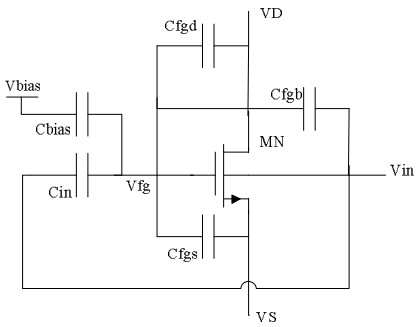

Fig 4. Bulk driven floating gate NMOST

In Fig. 4, the gate of MOST MN is converted in floating state using input capcitor $\left(C_{in}\right)$ and its other end connected to bulk so as to make it bulk controlled device. A large value biasing capacitor $\left(C_{bias}\right)$ is used at gate of MN to keep BDFG MOST in saturation mode. In DC condition, the BDFG performs as BD MOST whereas for AC it combines the characteristics of BD and FG MOST which results in effective

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transconductance higher than alone BD or FG MOST but remians below GD MOST.

Bulk Driven Quasi-floating Gate (BDQFG) MOSFET

The bulk-driven quasi-floating gate (BDQFG) MOST is similar to that of BDFG MOST, except the difference lies in gate-node potential. In BDQFG instead of applying gate to a fixed DC potential, it is configured in quasi-floating state. The structure overcomes the issues of BDFG MOST and hence got popularity in an exponential manner. The schematic of an N-channel BDQFG MOST along with its parasitic capacitances is shown in Fig. 5.

Likewise BDFG, BDQFG MOST is formed with the difference only in state of its gate potential which is changed in quasi-floating state via large value resistance $\left(R_{large}\right)$ of P-channel MOS transistor (MP) working in cut-off region. Moreover, absence of C_{bias} in BDQFG does improve the effective transconductance compared to BDFG and so the gain-bandwidth product. Under DC, the BDQFG performs as BD MOST whereas for AC it combines the characteristics of BD and QFG MOST which results in effective transconductance higher than alone BD or QFG MOST.

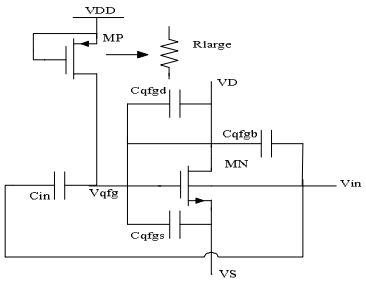

Fig 5. Bulk driven quasi-floating gate NMOST

It is worth here to be noted that the effective transconductance of BDQFG is almost equal to GD MOST which can be observed in [26] where experimental validation has been shown. Few recent articles reporting this approach in the design of current mirrors has been presented in [27-31].

Table I: Comparison of MOSFET Parameters [29]

Tech-niques	Threshold	Trans-conductance	Conduc-tance	Transitional frequency
GD	V_{th}	g_m	g_{ds}	f_T
BD	removed	$(0.2-0.4)\,g_m$	g_{ds}	$(0.3-0.5)\,f_T$
FG	$V_{th,eff} << V_{th}$	$(0.3-0.5)\,g_m$	$> g_{ds}$	$(0.4-0.6)\,f_T$
QFG	$V_{th,eff} << V_{th}$	$(0.5-0.6)\,g_m$	$> g_{ds}$	$(0.5-0.7)\,f_T$
BDQFG	removed	$(0.7-1)\,g_m$	$> g_{ds}$	$(0.7-0.9)\,f_T$

A comparison of performance parameters of GD, BD, and FG, QFG and BDQFG has been summarized in Table 1. Due to drawbacks associated with FG MOST, the BDFG technique does not achieved encouragement for circuit realization.

III. PROPOSED OTA

OTA is the VCCS device, used as versatile building blocks which offer wide bandwidth for many types of amplifiers. Based on BDQFG technique the schematic of proposed miller compensated OTA is shown in Fig. 6. The proposed OTA uses BDQFG input differential pair which results in enhanced transconductance of OTA.

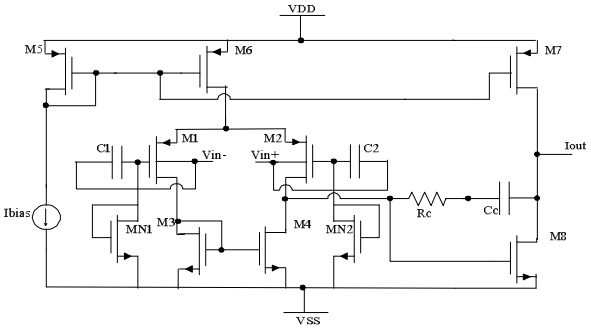

Fig 6. BDQFG based OTA

The improved gain of BDQFG OTA results in high UGB product given by

$$A_{0,proposed} = \left(kg_{m2} + g_{mb2}\right) g_{m8} \left(r_{02} // r_{04}\right)\left(r_{07} // r_{08}\right)$$

whereas the same OTA when realized using BD MOSFET, the UGB is given by

$$A_{0,BD} = g_{mb2} g_{m8} \left(r_{02} // r_{04}\right)\left(r_{07} // r_{08}\right)$$

As observed, the BDQFG OTA provides high gain and better UGB product as compared to BD OTA and maintains the same level of power consumption.

IV. SIMULATION RESULTS

The effect of aforementioned techniques on N-channel MOST (NMOST) performance parameters is shown with the help of HSpice simulations and compared to GD based NMOST. During simulation the NMOST taken have width and length on $100\,\mu m$ and $0.54\,\mu m$ respectively and considered to be working in saturation mode. The simulations have been achieved under the same environment using the MOSFET model of UMC $0.18\,\mu m$ technology at a supply of 0.5 volt.

The other assumed parameters include input capacitance $\left(C_{in}\right)$ and bias capacitance $\left(C_{bias}\right)$ of 1pf respectively along with MOST dimension of W/L=$0.36\,\mu m$ /$0.36\,\mu m$ used for realizing R_{large} wherever applicable. The plots include threshold voltage, transconductance, output resistance and transitional frequency. The plot of drain-to-source current of GD, BD, FG, QFG, BDFG and BDQFG is shown in Fig. 7. From plots it is quite clear that for BD approach the NMOST turns-ON in negative voltage and the same graph observed for BDFG and BDQFG since as stated earlier under DC

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conditions BDFG and BDQFG functions as simple BD NMOST.

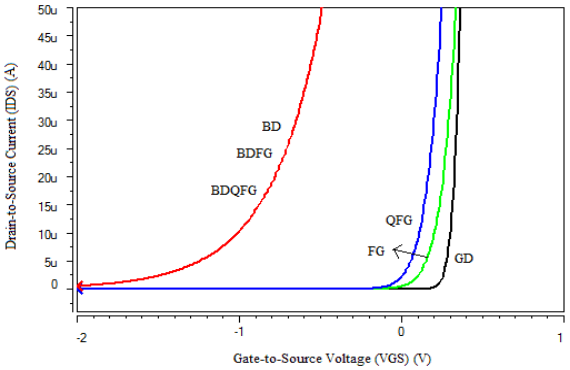

Fig 7. Input characteristics

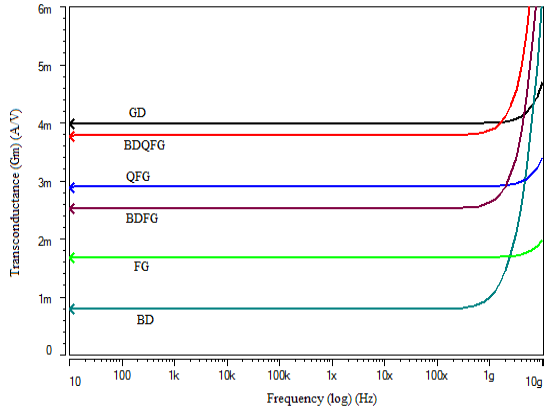

Fig 8. Transconductance plots

For FG and QFG, the current flow can be observed at smaller Vgs compared to GD which clearly indicate the low voltage requirements by the techniques. Similarly, the simulation of comparison of transconductance is shown in fig. 8. As observed the highest is observed in normal GD NMOST whereas in case of discussed techniques, the highest is observed for BDQFG NMOST followed by QFG and then BDFG, FG and lastly the lowest by BD NMOST. Likewise, the plot for output resistance and the transitional frequency is shown in fig. 9 and fig. 10 respectively. However, in Fig. 8, as observed the output resistance is degraded which is due to feedback capacitances. The HSpice simulation results of these parameters are shown in tabulated form in Table 2.

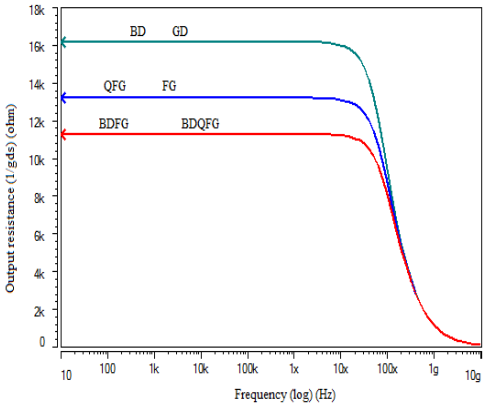

Fig 9. Output resistance plots

Form Table 2, it can be observed that considering the floating gate technology QFG provides comparable performance to GD. Alternatively, using BD the power consumption is reduced significantly but at the cost of poor dynamic range and poor performance parameters.

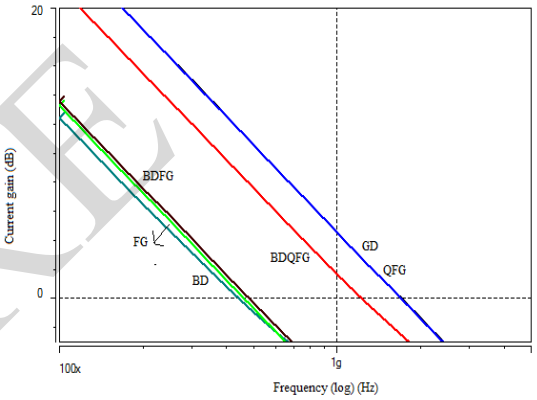

Fig 10. Current gain plot for calculating transitional frequencies

Table II: Comparative Analysis Of LV LP Techniques

Technique	Transconductance (uA/V)	Output resistance (ohm)	Transient frequency (Hz)
GD	4000	16K	1.7G
BD	800	16K	0.446G
FG	1700	13K	0.464G
QFG	2900	13K	1.7G
BDFG	2500	11K	0.480G
BDQFG	3800	11K	1.25G

However, this drawback got overcome using BDQFG approach which in addition to low power consumption provides enhanced performances over other LP techniques, i.e. almost similar to GD technique. The only drawback with BDQFG is the poor DC characteristics since under DC the behavior is identical to BD. So, it can be easily concluded that QFG and BDQFG techniques are the best solutions for design of LV LP analog circuits. Further the OTA parameter analysis on 0.18 μm mixed-mode twin-well technology provided by UMC with the help of HSpice is shown in summarized form in Table 3.

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Table III: Comparative analysis of BD and BDQFG OTA

Parameters	BD OTA	Proposed BDQFG OTA
Transconductance (G_m) $(\mu A/V)$	1700	7440
DC gain	40.9	53.81
Dominant pole (KHz)	87.8	87.1
UGB (MHz)	11.27	101.13
Phase Margin (PM)	114	65
Power (μW)	51.47	51.46
Output impedance $(K\Omega)$	117	117
Voltage Supply	$\pm$ 0.5V	$\pm$ 0.5V

V. CONCLUSION

From the discussed techniques, it can be concluded that using FG and QFG a comparable performance to GD can be achieved at low power. However, using BDQFG the frequency domain performances can be achieved almost similar to GD MOST with an added advantage of having low power consumption as shown with the help of OTA design.

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